UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

LINEAR TECHNOLOGY CORPORATION Plaintiff, v. MONOLITHIC POWER SYSTEMS, INC. Defendant.	)	C.A. No. 06-476 (GMS)

DECLARATION OF ROBERT A. BLAUSCHILD

I, ROBERT A. BLAUSCHILD, declare as follows:

1) My name is Robert A. Blauschild. I reside at 22351 Hartman Drive, Los Altos, CA 94024. I have been retained by Linear Technology Corporation (LTC) as an expert witness in this case.

2) Unless indicated as being on information and belief, the facts and opinions stated in this declaration are based on my own personal knowledge. If asked to testify in Court under oath about the matters discussed in the declaration, I could and would so testify.

I. QUALIFICATIONS

3) Since obtaining a B.S.E.E. degree from Columbia University in 1971 and an M.S.E.E degree from U.C. Berkeley in 1973, I have been involved in the design and analysis of analog and mixed-signal (analog + digital) electronic circuits and systems. I have worked as a consultant to numerous companies, in addition to having worked for Philips Semiconductors for 24 years. I have 15 patents, was on the program committee for the International Solid-State Circuits Conference for 15 years, and have twice been the guest editor of the Journal of Solid-State Circuits. I also have been involved as a testifying expert witness in several patent cases

relating to analog and digital circuit design. A copy of my current Curriculum Vitae is attached to this declaration as Exhibit 1.

4) I have designed numerous bipolar and MOS voltage and current references, voltage regulators, differential amplifiers, and amplifier output stages.

II. COMPENSATION

5) I am being compensated for my work in this case at my usual and customary consulting rate of $450 per hour. My compensation is not dependent on the outcome of the case.

III. PRIOR TESTIMONY

6) In the past four years I have testified at trial or at deposition in the role of an expert witness in the following matters on behalf of the underscored party:

2003 Presented a tutorial regarding transistor operation and switching voltage regulator design in court in Linear Technology vs. Micrel, Northern District of California.

2005 Testified in deposition and trial in Linear Technology vs. Micrel, Northern District of California.

2005 Testified in deposition, Linear Technology vs. Monolithic Power Systems, ITC, Washington D.C., regarding switching voltage regulator design.

2006 Testified in deposition and trial, Power Integrations vs. System General, ITC, Washington D.C., regarding switching voltage regulator design.

2006 Testified in deposition and at trial in Power Integrations vs. Fairchild Semiconductor, Wilmington, Delaware. The case involved switching voltage regulators and analog circuit design.

VI. LTC Burst Mode Patents

A. Overview of the LTC Burst Mode Patents

7) The discussion below describing the operation of the circuitry of the '178 patent also applies to LTC's '6,580,258' patent, which shares the same specification as the '178 patent.

8) The '178 patent relates to circuitry for controlling the operation of a synchronously switched switching regulator. A synchronously switched switching regulator uses two switching transistors that alternately turn on to supply current to a load.

9) The '178 patent describes circuitry and methods in which a synchronous switching regulator automatically switches between normal synchronously switched operation at high or moderate load currents, and alternating between switching and sleep mode operation at low load currents, thereby achieving improved efficiency over a wide range of load currents.

10) In addition, the '178 patent discloses circuitry and methods to solve the problem of reverse current flow previously associated with the use of synchronously driven switching transistors. By providing a solution to this problem, synchronously driven switching transistors could be used at low as well as high load currents, with or without the automatic sleep mode feature.

11) In a first state of operation, at heavy or moderate load current levels, the '178 system operates by generating a control signal to vary the duty cycle of the synchronously switched switching transistors to keep the output at the regulated voltage, controlled to be in a range about a nominal value. Both switches operate synchronously, providing high efficiency.

12) For example in the embodiment of Fig. 2 of the '178 patent, below a desired load current threshold level, when the output capacitor can supply current to the load to maintain the regulator output substantially at the regulated voltage for a period of time, both

switching transistors are turned OFF (second state of circuit operation), improving efficiency by saving the power needed to continuously turn both switching transistors ON and OFF. And with the bottom switch turned OFF, reverse current flow in the inductor is avoided. When the regulator voltage droops to a predetermined level, at least one of the switching transistors is turned ON again to recharge the output capacitor. If the load current remains below the threshold level, both switching transistors will then be turned off again. If the load current goes back up, the regulator returns to the first state of circuit operation. The output voltage in the second state of circuit operation is still regulated (controlled), but its range of variation may be larger than that achieved in the first state of circuit operation.

13) As described above, with synchronous switching, when instantaneous inductor current reverses, charge is pulled from the output capacitor and conducted to ground instead of to the load. The '178 inventors solved this problem by turning the bottom switching transistor OFF when a reverse polarity condition exists. Breaking the current path between the output circuit and ground prevents the flow of reverse inductor current. By turning off the switch when the inductor current is about to or has just crossed zero, inefficiency due to drawing charge back from the output capacitor is minimized, and drawing power from the load is prevented. A synchronous switching voltage regulator using the '178 control system can therefore achieve high efficiency at both high and low load current levels.

14) Based on my experience, a person of ordinary skill in the art would have either a BSEE or MSEE degree in electrical engineering, which would acquaint them with the basic equations for calculating voltages and currents in a circuit, including both dc and transient analysis based on the values of components such as resistors, inductors, and capacitors. Such a person would also have 3-7 years experience designing analog electronic circuitry in general, and

be familiar with the basic textbook topologies of switching power supplies (e.g., step-down, step-up, and inverting).

B. '178 Claim Construction Issues

15) Of the '178 cites provided by MPS in support of their proposed constructions, substantially all refer to the prior art Fig. 1 circuit or the embodiment of Fig. 2. In addition, MPS only identifies structures in the Fig. 2 circuit as being disclosed structure for '178 Claim 34. The claims of the '178 patent are not limited to the Fig. 2 circuit.

16) Independent Claim 1 clearly covers circuitry other than the step-down configuration of Fig. 2. The Fig. 2 circuit is a step-down switching regulator. This means that the input voltage is higher than the voltage at the load. [3:5-9; 5:44-48; 18:60-62] The Fig. 9 circuit is a step-up switching regulator. This means that the input voltage is less than the voltage at the load. [3:37-39; 18:65-67] Claim 32, which depends from Claim 1, further specifies that the circuit of Claim 1 is a step-up voltage regulator. An example of such a step-up switching regulator is the Fig. 9 circuit. The Fig. 9 circuit has all the same control circuitry for controlling its two synchronously switched switching transistors as the Fig. 2 circuit, arranged in the same way.

17) The Fig. 7 circuit is a more detailed schematic diagram of a step-down switching regulator. [12:1-6] The Fig. 7 circuit shows more detail of the one-shot timing circuitry for controlling the switching transistors. As with the Fig. 2 circuit, the Fig. 7 circuit also has a continuous mode of operation for high load currents and a sleep mode of operation at low load currents. [12:14-13:7] As with the Fig. 2 circuit, the Fig. 7 circuit switches between continuous operation (synchronous switching) and sleep mode automatically to provide high efficiency over a broad range of load currents, including low load currents. [8:1-16; 12:1-13:7]

18) A one-shot is a circuit that outputs a pulse once it is triggered by an input, and then returns to its original state where it remains until it is triggered again. The one-shot pulse width can be fixed (e.g., as shown in Fig. 2) or variable (e.g., as shown in Figs. 5 and 7).

19) Dependent Claims 14-17 claim details of the one-shot circuit, including timing dependency on inputs from the regulator input and output voltages. These claims ultimately depend from Claim 1, and therefore Claim 1 must cover more than a control circuit with the fixed time one-shot shown in the Fig. 2 control circuit.

20) I also agree with the *Impala* District Court's construction of "coupled" -- circuit elements are coupled when a current path exists between them. I note that MPS has proposed that "circuit elements are 'coupled' when they are so arranged that energy can transfer electrically or magnetically from one to another." I find no support in the '178 patent for such a construction, and MPS has not described what it means by "electrical connection" and "magnetic connection."

21) MPS construes a "load" to be "a device, circuit, or system that consumes electric power, not part of the regulator structure." I agree that a load is a device, circuit, or system, but I do not agree that it must consume electric power. It can consume electric power if current is supplied to it by the regulator. However, if the load's power requirement is shut off (for example, by turning off a switch in the load), the load would still be a device, circuit, or a system, and it would still be coupled to the regulator, but it would not be consuming electric power. I agree with the proposed LTC construction that a "load" is a device, circuit, or system coupled to the output terminal to which the regulator can supply current.

22) I disagree with the MPS proposed construction that "first state of circuit operation" is "a state in which the output voltage is maintained during high load current

conditions by switching the switching transistors in a complementary manner to provide power to the load." The switching transistors are synchronously switched. The patent states: *For example, at high output current levels during a first state of circuit operation the switch continually alternates between an ON state and an OFF state to maintain the output voltage V_{OUT} at the regulated voltage level V_{REG}.* [8:4-8] See also, for example, 5:59-6:16, contrasting the sleep mode state of operation in which both of the switching transistors are simultaneously OFF to a mode in which one of the two switching transistors is substantially ON at all times. I agree with the *Impala* District Court construction the "first state of circuit operation" is the state in which the switching transistors are both enabled for switching and are synchronously switched, such that one transistor is ON and the other is OFF, with a varying duty cycle to maintain a regulated voltage at the output terminal.

23) I disagree with the MPS proposal that the "second state of circuit operation" is "a state in which, as a result of low load current conditions, the output capacitor maintains the output voltage substantially at the regulated voltage, while the switching transistors are disabled." Claim 34 of the '178 patent does not contain the limitation of having the output capacitor maintain the output substantially at the regulated voltage, and the MPS proposed construction would add this extra limitation into that claim by including it in the construction of "second state of circuit operation."

24) I also disagree with the MPS proposed construction of a "threshold fraction of maximum rated output current" as being a fixed number. Such a construction would be inconsistent with the '178 patent. The *Impala* District Court did not include the requirement that the "threshold fraction" be "fixed" as MPS proposes. The threshold fraction can vary if output voltage ripple varies, as would happen if either a Pulse Width Modulator (PWM) or a

variable OFF-time control circuit were used. If the "threshold fraction" must remain "fixed" under all conditions, then such a construction would exclude circuits that use a Pulse Width Modulator instead of a Constant Off Time (COT) circuit like that of Fig. 2. The patent discusses the use of a PWM circuit as a direct substitute for the COT circuit. [9:12-22] Also, the Federal Circuit cited to the same discussion in the patent to determine that the PWM circuit was corresponding structure to the COT circuit. The patent also mentions COT circuits whose output varies with input voltage (V_{IN}). [9:23-27] Dependent Claim 14, which depends on Claim 7, which depends on Claim 1 specifically covers a COT circuit whose output can vary with input voltage.

25) I also disagree with MPS if, by construing a "switching voltage regulator" to require an "essentially constant" output voltage that they mean that the output voltage must be invariant. As explained in the patent, in the second state of circuit operation, the output voltage of the preferred embodiments varies as the output capacitor supplies charge to the load. [6:61-7:21] The patent also describes variation in the regulator output voltage in the first state of circuit operation. [4:24-30; 4:46-50]

26) The '178 patent describes circuitry and methods for controlling a switching voltage regulator. One of skill in the art would recognize that the regulator output voltage is not invariant, but is controlled in value, and that there will be some tolerance on the output voltage.

27) MPS has proposed construing "substantially at the regulated voltage" to mean "a voltage that has a different average value than the regulated voltage." There is no support in the '178 patent for this. To the contrary, one of skill in the art would understand from reading the specification that the regulator output voltage could have the same average output

voltage operating in the second state of circuit operation as it does in the first state of circuit operation. In the preferred embodiments of '178 Figs. 2 and 7, the output voltage levels in the second state of circuit operation are set by the upper and lower threshold voltages of hysteretic comparator 74. [7:6-17] The upper level of output voltage in the second state is above the regulated voltage V_{REG} [6:55-58], and the lower level of output voltage in the second state is below the regulated voltage level. [7:10-15] The amount of second state output voltage swing above and below the regulated voltage V_{REG} is determined by the amount of hysteresis in comparator 74. [6:64-7:5; 7:15-17] There is no limitation specified on the exact comparator thresholds, or the level of hysteresis. If the comparator thresholds are chosen to correspond to output voltages above and below the regulated voltage V_{REG} by the same amounts, then the average output voltage in the second state will be exactly the same as the average output voltage in the first state of circuit operation.

28) One of skill in the art would recognize that the second state of circuit operation need not be triggered by an output voltage level higher than an output voltage level maintained in the first state of circuit operation. The patent states: *the sleep mode control signal could be generated in response to a monitored output current.* [16:10-11]

29) One of skill in the art would also recognize that switching need not be resumed when the output voltage level has dropped any particular amount. The patent states: *Furthermore, the switching regulator could be taken out of the sleep mode a predetermined time period after going into such a mode, instead [off] after the output voltage falls below a predetermined threshold voltage, as illustrated above.* [16:12-16]

30) The level of output voltage variation need not be greater in the second state of circuit operation than in the first state of circuit operation. This is clearly demonstrated

by the discussion of the alternatives to triggering the beginning and end of sleep mode operation as opposed to the use of a hysteretic comparator. I agree with the District Court construction in the Impala litigation that "substantially at the regulated voltage" allows for, but does not require, greater variation in the voltage having a controlled value. [CCO, pp. 25-26]

31) The disclosed structures for generating a voltage feedback signal indicative of the voltage at the output [first means of Claim 34 of the '178 patent] include: a resistor divider [e.g., Figs. 2, 7, 8, and 9], with or without an operational amplifier [e.g., Fig. 10], or other conventional voltage feedback circuits [e.g., Fig. 5].

32) The disclosed structures for generating a first control signal ... responsive to the voltage feedback signal to vary the duty cycle ...[second means of Claim 34 of the '178 patent] include: drive circuit 20, transconductance amplifier 38, offset voltage V_{OS} 76, reference voltage 37, current comparator 39, a feedback current path between inductor L1 32 and current comparator 39, and a constant off-time one-shot circuit 25, which outputs the first control signal [Fig. 2]; or combinations having a pulse-width modulator circuit or a variable-off-time one-shot circuit [e.g., Fig. 5; 9:12-21; 10:11-16]; or the combination of resistors R_{SENSE} and R_3, reference voltage V_{REF}, offset voltage V_{OS}, current comparator 39, amplifier 38, one shot circuit 245, off-time controller 250, and capacitor C_{CON} [Fig. 7].

33) The disclosed structures for generating a second control signal ... [third means of Claim 34 of the '178 patent] include: as illustrated in Fig. 2, hysteretic comparator 74, V_{REF}, current source I1 72, and logic gates 66, 68, and 69 [6:34-46]; or as illustrated in Fig. 7, hysteretic comparator 74, current source I1 72, comparator 315, gate 316, V_{REF}, and related sleep control logic [12:46-13:2]; or combinations such as those disclosed at 16:5-12.

34) I disagree with MPS that a "selected sleep mode current level" represents a percentage of maximum rated output current. The plain claim language says that it's just a level, not a percentage of anything. The '178 patent states: *In accordance with the present invention, regulator circuit 50 goes into sleep mode at low output current levels as follows.* [6:34-36] I agree with the LTC construction that the "selected sleep mode current level" is a current level below which the regulator enters into a second mode of operation.

35) MPS proposes that a pair of switching transistors are "synchronously switched" when they are "driven out of phase to supply current at a regulated voltage to a load." MPS further specifies that "driven out of phase" means that the two switching transistors do not turn on and off at the same time at all times. Those of skill in the art know that there are two well known meanings of two transistors being "driven out of phase." The first meaning is that the transistors are alternately switched on and off so that one is on while the other is off. They are driven in an opposite manner. One or the other of the two transistors is on substantially at all times (except for a brief deadtime during the transition time when one transistor turns off and the other turns on). This is the meaning of "driven out of phase" that fits with the '178 patent. [3:66-4:18; 5:66-6:2; 6:17-19] The second well-known meaning of "driven out of phase" refers to two transistors that are not "in phase," meaning that they are not switched in the same manner. That is, they don't both turn on at the same time, stay on for the same amount of time, and then both turn off at the same time. This meaning of "driven out of phase" does not fit with the '178 patent. For example, both switching transistors could be simultaneously on for 90% of a switching cycle, and still MPS's construction could be met as long as they don't turn on and off exactly at the same time. The '178 patent teaches to avoid such a condition where the ON times of the two switching transistors overlap. [5:33-43] This can be done by having one of the

switching transistors ON and the other OFF, in an alternating manner, consistent with the above first well known meaning of driven out of phase.

36) Claim terms discussed above with respect to the '178 patent should be construed the same when they are used in the '258 patent. In the discussion below about disputed '258 patent claim terms, the cite given is from the '178 patent, which shares the same specification.

C. '258 Claim Construction Issues

37) I disagree with the MPS proposed construction of a "threshold" as being a fixed value. Such a construction would be inconsistent with the '178 patent. For example, the threshold for comparator 39 in the Fig. 1, 2, 7, and 9 circuits is described as varying with load current (e.g., *As the output load current increases, the voltage drop across R2 resistor 36B will decrease. This translates into a small error voltage at input 38B of transconductance amplifier 38 that will cause 38A to increase, thus setting a higher threshold for current comparator 39.* [4:47-50]).

I declare under penalty of perjury that the foregoing is true and correct.

Dated: June 8, 2007

Robert A. Blauschild

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on June 8, 2007 I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Richard L. Horwitz
POTTER ANDERSON & CORROON LLP

I also certify that copies were caused to be served on June 8, 2007 upon the following in the manner indicated:

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EXHIBIT 1

Resume of Robert Blauschild

I have worked extensively in the field of analog and mixed-signal circuit design. After presenting two technical papers at the 1978 International Solid-State Circuits Conference (ISSCC), I was chosen by the 1979 conference chairman to serve on the ISSCC Program Committee, and have been similarly chosen 15 times since then. I was twice a member of the European Solid-State Circuits Conference Program Committee. My work on these committees consisted of evaluating submitted papers for originality and import, and deciding on rejection or acceptance for presentation at the conferences.

After obtaining a BSEE degree from Columbia University in 1971 and an MSEE degree from U.C. Berkeley in 1973, I joined the Analog Research Department of Signetics. I became Manager of Analog Research in 1976, with a department charter to investigate the application of new process technologies to analog functions.

My status with Signetics became that of a consultant in 1981, which allowed me to work with other companies including Hughes, MicroLinear, Exar, Stanford Telecom, and many others. I rejoined Signetics as Manager of Advanced Development in 1990.

The charter of my department was to do advanced designs with existing IC processes, the first designs with new IC processes, and consult with other departments on the development of all projects with analog content. We were also responsible for working with the wafer fabrication groups in developing new IC processes and devices.

I have participated as a panelist at various industry conferences, and taught several short courses and seminars in the U.S., Europe, and Japan. My designs and lectures have spanned a wide range of technologies, including NMOS, CMOS, BiCMOS, and Bipolar processing.

I have worked on and consulted on designs of a wide range of analog and mixed-signal circuits, including data converters, amplifiers, voltage and current references and regulators, timing circuits, line drivers and receivers, display circuits, phase-locked loops, and modems.

I have fifteen US patents and have designed over two dozen products with cumulative sales above $250 Million.

Robert A. Blauschild Educational Background and Professional Activities

Educational Background

1967-71	Columbia University	(BSEE)
1971-73	UC, Berkeley	(MSEE)

Work Experience

2005 - present	Consultant (Ikanos/MySource Communications/Winbond)
2004	Consultant (Ikanos/line driver design)
2000 - 2004	Ikanos Corporation (Circuit Design for DSL Communications Chips)
1997 - 1999	Consultant (Philips/ CDMA cellphone chip and Ikanos Communications/data communications boards and chip design)
1973 - 1997	Signetics Corporation (Philips Semiconductors)
1973	Member of Analog, Research Department
1976	Manager of Analog Research
1981	Consultant / Manager of Analog Research Department
1990-1997	Manager of Advanced Development
1981-1989	Design Consultant (Signetics, Micro Linear, Exar, Hughes, SSI, et. al.) doing analog and mixed signal product design including data converters, amplifiers, PLLs, data communications, voltage references and regulators.

Product Development

Primary Design Responsibility

NE520S High-frequency Amplifier
NE5211, NE5212 High-speed Fiberoptic Preamps
NE5224, NE5225 Fiberoptic Post-Amplifiers
NE5080, KE5081 FSK Modem Chip Set
NE5180, NE5181 Octal RS232/433 Line Receivers

NE5170 Octal RS232/433 Line Driver
NE568A 150MHz PLL
Several High-volume Automotive custom circuits for engine control,
anti- lock braking, and display systems
L272 Dual Op amp

Design Contributions

NE5210 Fiberoptic Preamp
NE3842 SMPS Controller

NE7025 1GHz Low-voltage Frequency Synthesizer
CD8360 CDMA Baseband Chip for Cellular Phones
NE660 Low-voltage Dolby Processor
NE569 Video CRT Driver
NE5230 Op amp
High-Voltage Ballast Controller
Various Bandgap Voltage References for Large Digital Chips
EEPROM Voltage Reference and Programmer Supply
Multi-channel IR Signal Processor
Automotive Bus Transceiver

Supervision of Development

NE5206 High-frequency Power Amplifier
NE5222 Fiberoptic Preamplifier
NE5214, NE5217 Fiberoptic Post-amplifiers
NE5209 Wideband Variable-Gain Amplifier
Switched-Mode Ballast Controller

Circuit Design Consulting Areas

Amplifiers
Line Drivers and Receivers
Voltage References
Linear and Switching Voltage Regulators
Phase-Locked Loops
Codecs and Modems
Oscillators

Professional Activities

ISSCC Program Committee (16 times, Analog Sub-committee Chair in 1984)

ESSIRC (European Solid-State Circuits Conference) Program Committee

Guest Editor of the Journal of Solid-State Circuits (1980 and 1986)

ISSCC Panel Organizer and Participant (4 times)

Panelist at Wescon and Custom Integrated Circuit Conferences

6 ISSCC Presentations

7 Journal of Solid-State Circuits Papers

Short Courses Developed and Taught

High-speed Analog Design

High-frequency Phase-locked Loops

Signal Amplification and Gain Control in Disk Drives

High-frequency PLLs for Disk Drives

Practical Examples of PLLs for Transceiver

Parasitic Effects In High-Frequency ICs

Transistor-Level Design of an Off-Line SMPS Controller

Technical Publications

High-voltage Analog Performance with Low-voltage Digital Devices, Journal of Solid-State Circuits, Dec. 1978

A New NMOS Temperature-Stable Voltage Reference, Journal of Solid-State Circuits, Dec. 1978

An Open-loop Programmable Amplifier with Extended Frequency Range/Journal of Solid-State Circuits, Dec. 1981

A Four-Terminal Wide-band Monolithic Amplifier, Journal of Solid-State Circuits, Dec. 1981

A 14-bit PCM DAC, Journal of Solid-State Circuits, Dec. 1982

An 8-bit, 50nsec A/D, Digest of Technical Papers, 1983 International Solid-State Circuits Conference

Fleetest FSK Modem Chip-set Goes the Distance, Electronic Design, August 14, 1983

A Wide-band Low-noise Monolithic Transimpedance Amplifier, Journal of Solid-State Circuits, August 1986

A Wide-band Class-B Video Output Driver, Digest of Technical Papers, 1989 International Solid-State Circuits Conference

“Understanding Why Things Don’t Work”, Analog Circuit Design - Art, Science, and Personalities, Butterworth-Heinemann, 1991, pp. 123-126

An Integrated Time Reference Digest of Technical Papers, 1994 International Solid-State Circuits Conference